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ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	Application No.	Applicant(s)
Office Action Summary	10/736,125	PAI ET AL.
	Examiner	Art Unit	
	CHENG-YUAN TSENG	2184	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>12 September 2008</u>.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>18-28</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>18-28</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>12/15/2003</u> is/are: a)☐ accepted or b)☒ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

DETAILED ACTION

Response to Amendment

1.   The objections to drawings, claims, and rejections made
under Double Patenting, 35 U.S.C. 112 have <u>NOT</u> been withdrawn
due to the amendment filed on September, 12, 2008.   No response
regarding to those objections and rejections has been received.

Drawings

2.   The drawings are objected to as failing to comply with 37
CFR 1.84(p)(5) because they do **not include the following
reference signs mentioned in the description:**

In para. 0019, lines 1-2, the video data 305 is not shown
in figure 1.

In para. 0019, line 5, the pixels 315 is not labeled in
figure 1.

In para. lines 14-17, the packetized elementary sequence
360 and the transport header 365a are not shown in figures.

In para. 0021, lines 1-2, the transport packers 345b is not
found in figure 1.

In para. 0024, lines 4-10, the video elementary stream 355
is now shown in figure 2.

In para. 0025, line 2, the video data 305 is not shown.

3.   The drawings are objected to as failing to comply with 37

CFR 1.84(p)(5) because they include the following **reference**

characters not mentioned in the description:

      In fig. 2, there is no description on 470.

      In fig. 4, there is no description on circuitry 550 and

port 560.

      In fig. 5, there is no description about the MUX 555(0)-

555(31).

      In fig. 5, there is no description about the port 560.

4.   The drawings are objected to because of following

informalities:

      In fig. 5, it is unclear if the 611 is connected to input

of MUX 555(1).

      In fig. 6, block 730, it is unclear the logic of the

flowchart. In particular, the 730 is a binary decision block.

There is no condition leading to END.

      In fig. 6, there should be an arrow from block 730 to block

735.

Claim Objections

5.   Claim 19 is objected to because of the following

informalities:

As to claim 19, claim must end with period.

Double Patenting

6.   The nonstatutory double patenting rejection is based on a

judicially created doctrine grounded in public policy (a policy

reflected in the statute) so as to prevent the unjustified or

improper timewise extension of the "right to exclude" granted by

a patent and to prevent possible harassment by multiple

assignees.   A nonstatutory obviousness-type double patenting

rejection is appropriate where the conflicting claims are not

identical, but at least one examined application claim is not

patentably distinct from the reference claim(s) because the

examined application claim is either anticipated by, or would

have been obvious over, the reference claim(s). See, e.g., *In re*

Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re*

Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re*

Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van*

Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422

F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418

F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37

CFR 1.321(c) or 1.321(d) may be used to overcome an actual or

provisional rejection based on a nonstatutory double patenting

ground provided the conflicting application or patent either is

shown to be commonly owned with this application, or claims an

invention made as a result of activities undertaken within the

scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent

of record may sign a terminal disclaimer. A terminal disclaimer

signed by the assignee must fully comply with 37 CFR 3.73(b).

7.   Claim 18 is rejected on the ground of nonstatutory

obviousness-type double patenting as being unpatentable over

claim 9 of U.S. Patent No. 7,284,072, hereinafter referring to

as Pat'072. Although the conflicting claims are not identical,

they are not patentably distinct from each other because of

following comparisons. Claim 18 is considered obviousness,

because it is claiming the same DMA controller as in Pat'072

with broader scope.

Claim 18 is comparing to claims 9 of Pat'072 in the

following table:

Instant Application	Pat'072
(claim 18) **a direct memory access controller, said direct memory access controller** comprising:	(claim 9) **a system for providing a plurality of sequential data words, said system** comprising:
a state logic machine for receiving **a single command** to **provide a specific range of a plurality of sequential data words;** and	**a state logic machine** for receiving **a command** to **provide the plurality of sequential data words,** wherein …
a memory controller for **fetching a first portion** of the range and **a second portion** of the range after fetching the first portion, wherein the second portion of the range has **a lower address than the first portion, after the state logic receives the single command.**	**a memory controller** for **fetching a sequential portion** of the sequential data words, said sequential portion comprising **a first intermediate word, the last word, and one or more data words between the intermediate word and the last word;** …

Claim Rejections - 35 USC § 112

8.   The following is a quotation of the second paragraph of 35

U.S.C. 112:

> The specification shall conclude with one or more claims particularly
> pointing out and distinctly claiming the subject matter which the applicant
> regards as his invention.

9.   Claims 24-27 are rejected under 35 U.S.C. 112, second

paragraph, as being indefinite for failing to particularly point

out and distinctly claim the subject matter which applicant

regards as the invention.

   Claim 24 recites the limitation **"the** predetermined amount"

in line 9.   There is insufficient antecedent basis for this

limitation in the claim.

   As to claims 25-27, they are depending on claim 24.

Therefore, they are rejected as set forth above accordingly.

Claim Rejections - 35 USC § 102

10.   The following is a quotation of the appropriate paragraphs

of 35 U.S.C. 102 that form the basis for the rejections under

this section made in this Office action:

> A person shall be entitled to a patent unless - (a) the invention was known
> or used by others in this country, or patented or described in a printed

> publication in this or a foreign country, before the invention thereof by the
>
> applicant for a patent.

11. Claims 18-27 are rejected under 35 U.S.C. 102(a) as being

anticipated by Lee (U.S. Patent 6,842,219), hereinafter

referring to as Lee'219.

     Referring to claim 18, Lee'219 discloses **a direct memory**

access controller (fig. 2, VDEC 203), said direct memory access

controller comprising:

     a state logic machine (fig. 4, state machine 404; and fig.

12, FSM 1206) for receiving **a single command** (fig. 5, control

command 501; and fig. 6, command 601) to provide **a specific**

range (col. 11, lines 15-19, address range of external memory to

be accessed) of **a plurality of sequential data words** (col. 4,

lines 24-29, accessed memory blocks has plurality of sequential

data words); and

     a memory controller (fig. 11, buffer controller 1113) for

fetching **a first portion** (fig. 11, portion of VLD input buffer

1112) of the range and **a second portion** (fig. 11, portion of VLD

input buffer 1112) of the range after fetching the first

portion, wherein the second portion of the range has **a lower**

address than (col. 10, lines 49-55, backward decoding; col. 15,

lines 49-52, MPEG-4 rewinding, earlier frame has lower memory

address) the first portion, after the state logic receives the

single command.

Referring to claim 24, Lee'219 discloses a method for

fetching data words, said method comprising:

receiving a single command (fig. 5, control command 501;

and fig. 6, command 601) to provide **a specific range** (col. 11,

lines 15-19, address range of external memory to be accessed) of

a plurality of sequential data words (col. 4, lines 24-29,

accessed memory blocks has plurality of sequential data words),

starting **a beginning address** (col. 10, lines 49-55, backward

decoding process, earlier packets) and ending at **an ending**

address (col. 10, lines 49-55, backward decoding process, later

packets);

fetching a portion (col. 6, lines 58-60, words), in **a**

forward address order (col. 13, lines 33-35, increased address),

of the range of **sequential data words** (col. 13, lines 33-35, bit

stream), said wherein said portion of the range of sequential

data words consists of [the]**a predetermined amount of data words**

(col. 6, lines 58-60, four words) that conclude with and precede

the ending address, and wherein the predetermined amount of data

words is equivalent to **a capacity of a local buffer** (fig. 16,

DBC MEM);

fetching, in the forward address order, at least one preceding portion (col. 13, lines 33-35, increased address) of the range of sequential data words, wherein each of the preceding portions of the range of sequential data words consist of the predetermined amount of data words; and

wherein **a one of the preceding portions** (col. 10, lines 49-55, backward decoding; col. 15, lines 49-52, MPEG-4 rewinding and error resilience, the point of error has beginning address) of the range of sequential data words comprises the beginning address, truncating those data words that precede the beginning address.

As to claim 19, Lee'219 discloses the direct memory access controller of claim 18, wherein the memory controller fetches the first portion of the range and the second portion of the range in **a forward address order** (col. 13, lines 33-35, increased address).

As to claim 20, Lee'219 discloses the direct memory access controller of claim 18, further comprising: **a local buffer** (fig. 16, DBC MEM) for storing the first and second portions in **a forward address order** (col. 13, lines 33-35, increased address),

said local buffer comprising **a plurality of data words** (fig. 16,

DBC MEM, four words).

     As to claim 21, Lee'219 discloses the direct memory access

controller of claim 20, wherein the plurality of data words of

the local buffer are **narrower in width** (fig. 16, DBC MEM with 16

bytes vs. input stream in words) than the sequential data words.

     As to claim 22, Lee'219 discloses the direct memory access

controller of claim 20, further comprising: **a port** (fig. 12,

PMU IN) for transmitting the contents of the plurality of data

words of the local buffer in **a reverse address order** (fig. 12,

reversal logic).

     As to claim 23, Lee'219 discloses the direct memory access

controller of claim 22, further comprising: **at least one**

multiplexer (fig. 12, multiplexers inside 1203) for reversing

the bit positions of contents of **at least one of the data words**

(fig. 12, B DO[31:0]) of the local buffer.

     As to claim 25, Lee'219 discloses the method of claim 24,

further comprising: **loading** (fig. 12, load into CLUST DEC 1202)

the portion and the at least one preceding portions of the
sequential data words into the local buffer.

As to claim 26, Lee'219 discloses the method of claim 25,
further comprising: **reversing** (fig. 12, reversal logic) the
portion and the at least one preceding portions of the range of
sequential data words.

As to claim 27, Lee'219 discloses the method of claim 26,
further comprising: **reversing** (col. 10, lines 49-55, backward
decoding; col. 15, lines 49-52, MPEG-4 rewinding and error
resilience, the point of error has beginning address) the
truncated one of the preceding portions of the range of
sequential data words that comprises the beginning address.

As to claim 28, Lee'219 discloses the direct memory access
controller of claim 18, wherein the first portion and the second
portion are **adjacent to each other** (fig. 14, bit stream forms
the first/second portions, stream has adjacent bits).

Response to Arguments

12. Applicant's arguments filed on September 12, 2008,

regarding the 35 U.S.C. §102 have been fully considered, but

they are not deemed to be persuasive.

Applicants argue that the cited prior art does not disclose

amended independent claims in "fetching … a second portion of

the range after fetching the first portion, wherein the second

portion of the range has a lower address than the first portion"

and "a single command to provide a specific range of plurality

of sequential data words", because Applicants only grasp the

figs. 5 and 6 as a view illustrating the structure of a

coprocessor operation control command that controls a CODEC

block in DSCU described in fig. 6.

Examiner respectfully disagrees with Applicants, because

Lee'219 expressively discloses the command 601 contains fields

such as CRd to select external memory as first range, internal

DEC memory as second range, and local memory as third possible

range as disclosed in col. 11, lines 20-36. It is also noted

that the data for CODEC are known as "streaming data", therefore

the first and second portions are always adjacent while

streaming, regardless reading the data in forward or backward.

Conclusion

13. **This action is made final.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire in three months from the mailing date of this action. In the event a first reply is filled within two months of the mailing date of this final action and the advisory action is not mailed until after the end of the three-month shortened statutory period, then the shortened statutory period will expire on the date of the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than six months from the date of this final action.

Contact Information

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cheng-Yuan Tseng whose telephone number is (571)272-9772. The examiner can normally be reached on 09:00-16:00 Monday-Thursday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dr. Henry Tsai can be reached on

(571)272-4176. The fax phone number for the organization where

this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be

obtained from the Patent Application Information Retrieval

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may be obtained from either Private PAIR or Public PAIR. Status

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like assistance from a USPTO Customer Service Representative or

access to the automated information system, call 800-786-9199

(IN USA OR CANADA) or 571-272-1000.

/CT/

Patent Examiner, AU 2184

/Henry W.H. Tsai/

Supervisory Patent Examiner, Art Unit 2184